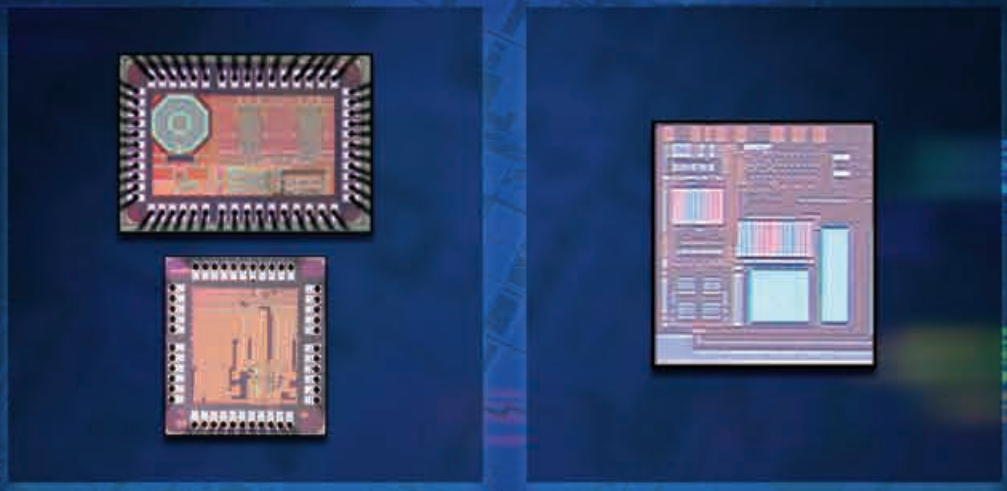

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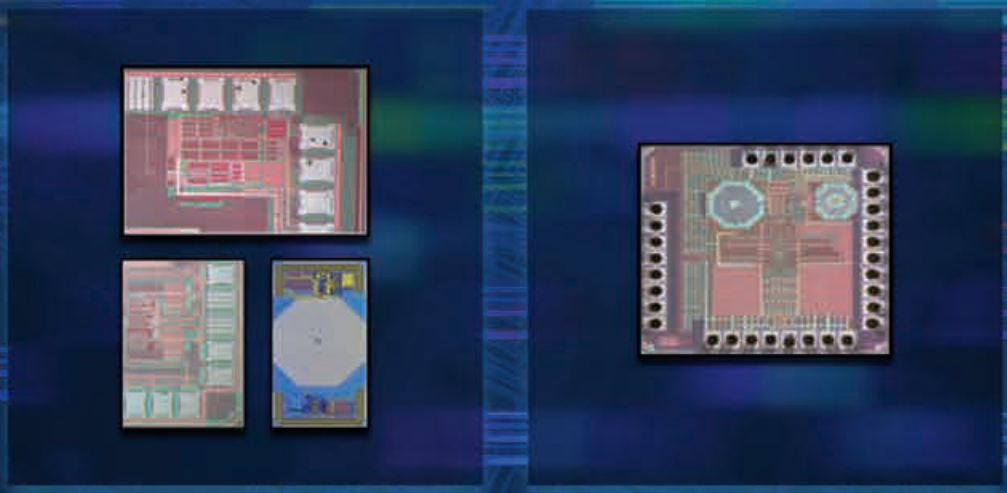
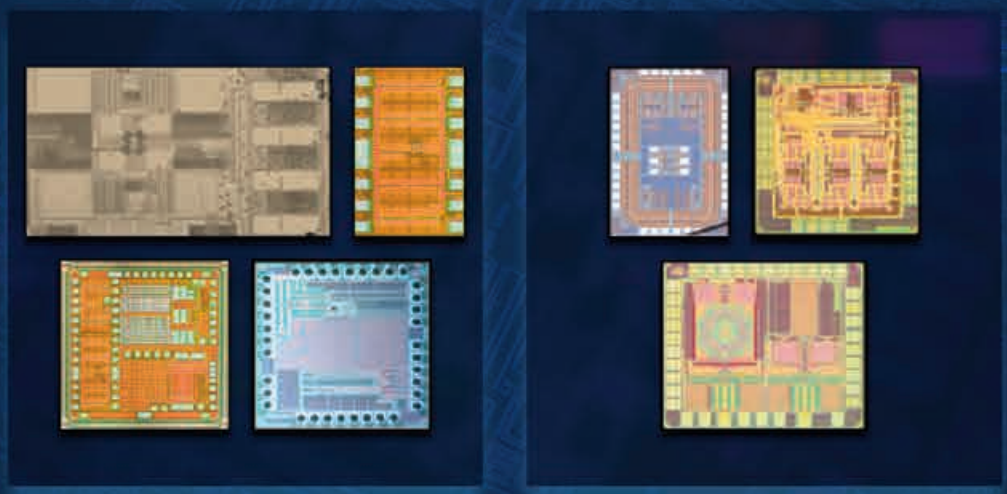




ISSCC 2011

1. A 0.46mm² 4-dB NF Unified Receiver Front-End for Full-Band Mobile TV in 65nm CMOS
2. A 0.024mm² 8-bit 400 MS/s SAR ADC with 2-bit per Cycle and Resistive DAC in 65nm CMOS

ISSCC 2012

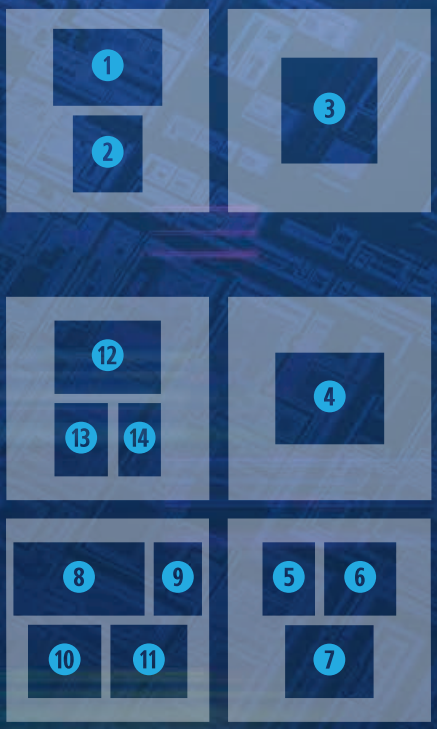
3. A 0.016mm² 144μW Three-Stage Amplifier Capable of Driving 1-to-15nF Capacitive Load with >0.95MHz GBW

ISSCC 2013

4. A 1.7mW 0.22mm² 2.4GHz ZigBee RX Exploiting a Current-Reuse Blixer+Hybrid Filter Topology in 65nm CMOS

ISSCC 2014

5. A 0.0013mm² 3.6μW Nested-Current-Mirror Single-Stage Amplifier Driving 0.15-to-15nF Capacitive Loads with >62° Phase Margin
6. An RF-to-BB-Current-Reuse Wideband Receiver with Parallel N-Path Active/Passive Mixers and a Single-MOS Pole-Zero LPF
7. A 0.5V 1.15mW 0.2mm² Sub-GHz ZigBee Receiver Supporting 433/860/915/960MHz ISM Bands with Zero External Components



ISSCC 2015

8. A 5.5mW 6b 5GS/s 4×-Interleaved 3b/cycle SAR ADC in 65nm CMOS
9. A 2-/3-Phase Fully Integrated Switched-Capacitor DC-DC Converter in Bulk CMOS for Energy-Efficient Digital Circuits with 14% Efficiency Improvement
10. A 123-Phase DC-DC Converter-Ring with Fast-DVS for Microprocessors
11. A 0.028mm² 11mW Single-Mixing Blocker-Tolerant Receiver with Double-RF N-Path Filtering, S_{11} Centering, +13dBm OB-IIP3 and 1.5-to-2.9dB NF

ISSCC 2016

12. A 0.038mm² SAW-less Multi-Band Transceiver Using an N-Path SC Gain Loop
13. A 0.003mm² 1.7-to-3.5GHz Dual-Mode Time-Interleaved Ring-VCO Achieving 90-to-150kHz $1/f^3$ Phase Noise Corner
14. A Handheld 50pM-Sensitivity Micro-NMR CMOS Platform with B-Field Stabilization for Multi-Type Biological/Chemical Assays

ISSCC: IEEE International Solid-State Circuits Conference

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